

CLAIMS

1. (Amended) A power supply device comprising:

5 a capacitor unit in which capacitors are interconnected in series or  
in series-parallel;

a charging unit for charging the capacitor unit at a constant  
current;

a detecting unit for detecting voltage on a high potential side of  
each capacitor;

10 a determining unit for determining existence of an abnormality by  
performing calculation based on the voltage detected by the detecting unit; and

a communication unit for outputting a determining result from the  
determining unit,

wherein

15 the determining unit determines the abnormality when  
difference between respective voltages on the high potential side of some  
adjacent capacitors exceeds upper-limit voltage "Va", when the difference is  
lower than lower-limit voltage "Vb", or when a voltage value is negative, and

20 the determination is not performed just after start of the  
charge of the capacitors, and the determination is started at the time when  
charge voltage Vc of the capacitor unit is at most a predetermined voltage value  
"Vd".

2. (Cancelled)

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3. The power supply device according to claim 1,

wherein lower-limit voltage value "Vb" is expressed by

$$V_b = V_c / (2N),$$

where “V<sub>c</sub>” is a charge voltage value of the capacitor unit and “N” is series number of the capacitors.

5           4. The power supply device according to claim 1,

          wherein the determination is started at the time when a charge voltage value of the capacitor unit is at most a predetermined voltage value.

5. (Amended) The power supply device according to claim 1,

10           wherein the predetermined voltage value “V<sub>d</sub>” is expressed by

$$V_d = V_t \times \{ 1 + (N - 1 - M) \times (1 - \text{dev}) / (1 + \text{dev}) \} - \alpha,$$

where “V<sub>t</sub>” is a withstand voltage value per capacitor cell, “dev” is a capacity variation of the capacitors, “N” is series number of capacitors, “M” is the number of series stages including short-failed capacitors, and “α” is a detection  
15 error margin.